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Applicants: Chen-Chih HUANG et al.

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) **VERIFIED TRANSLATION**
) **OF**
) **PRIORITY DOCUMENT**

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PO Box 1450
Alexandria, VA 22313-1450

Sir:

Chi-Fai Chung, whose office address is

22F-2, No. 510, Chung-Hsiao E. Rd., Sec. 5, Taipei City 110, Taiwan, R.O.C., declares that:

1. He knows well both the Chinese and the English languages;
2. He prepared the attached English translation of Taiwanese Patent Application number 90104097, filed February 22, 2001; and
3. He verifies that the attached English translation is an accurate translation to the best of his knowledge and belief.

He further declares that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

Signed this sixth day of May, 2008.

Chi-Fai Chung

Application Date:	Application No:
IPC classification:	

(The above fields are to be filled in by the Patent Office)

SPECIFICATION OF INVENTION	
I. TITLE OF INVENTION	Phase-interpolation circuit and a phase-interpolation signal generating device applying the same
II. INVENTORS	<p>NAME: 1. Chen-Chih Huang</p> <p>2. Pao-Cheng Chiu</p> <p>NATIONALITY: 1. Taiwan, Republic of China (R.O.C.)</p> <p>2. Taiwan, Republic of China (R.O.C.)</p> <p>ADDRESS:</p> <p>1. No 2, Industry E. Road, IX, Science-Based Industrial Park, Hsinchu</p> <p>2. No 2, Industry E. Road, IX, Science-Based Industrial Park, Hsinchu</p>
III. APPLICANT	<p>NAME: 1. Realtek Semiconductor Corp.</p> <p>NATIONALITY: 1. Taiwan, Republic of China (R.O.C.)</p> <p>ADDRESS: 1. No 2, Industry E. Road, IX, Science-Based Industrial Park, Hsinchu</p> <p>Representative: 1. Po-Ren Yeh</p>

IV. CHINESE ABSTRACT OF THE DISCLOSURE (TITLE OF THE INVENTION: Phase-interpolation circuit and a phase-interpolation signal generating device applying the same)

5 The invention relates to a phase-interpolation circuit and a phase-interpolation signal generating circuit applying the phase-interpolation circuit. The phase-interpolation circuit can avoid short-circuit current effectively. In addition, the phase-interpolation circuit can interpolate an inter-phase signal between a rising edge and a falling edge of a clock pulse. The phase-interpolation signal generating device can generate multiphase
10 clock signals that not only have linearly distributed phases but also maintain good 50% duty cycle of the multiphase clock signals.

ENGLISH ABSTRACT (TITLE OF THE INVENTION:)

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This invention of the application has been applied for patent

in the country(region) _____with application date_____and application
No. _____. Does the application claim priority?

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NONE

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The microorganism related to the application has been stored in _____with the
date of storage_____and storage number _____.

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NONE

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V. DESCRIPTION OF INVENTION (1)

[Translator's note: The above indicating description "V. DESCRIPTION OF INVENTION (1)", where "(1)" indicates the page number of the section of the Chinese "description of invention", will be omitted in the following translation for the sake of brevity.]

FIELD OF THE INVENTION

The present invention relates to a phase-interpolation signal generating device and particularly to a phase-interpolation signal generating device which can avoid short-circuit current and generate linearly distributed phase-interpolation signals.

BACKGROUND OF THE INVENTION

Multiphase systems are widely applied in the data-recovery systems and the phase-lock loop circuits. The multiphase systems are also a main trend of design in the communication systems nowadays.

In a conventional data recovery system, after applying the equalizer to recover high frequency decayed signals resulting from noise of communication media and signal decay, the correct sampling of data streams still depends on the correct clock pulse. In addition, the rising/falling edges of the clock pulses need to be in the middle of the period of data in order to sample the data correctly. The conventional data recovery system uses a phase-lock loop circuit to achieve the clock-recovery in order to have correct received data stream and correct sampling clock pulses. However, several disadvantages exist when the phase-lock loop circuit is used for recovering the clock-pulse. (1) The first one is longer lock time. The function of

rectifying the phase by the phase-lock loop circuit is to accelerate or slow down the phase by converting the comparison result between a reference frequency (i.e. the received data stream) and the output of a voltage-controlled oscillator into a voltage signal and feeding the voltage signal back to the input of the voltage-controlled oscillator. In other words, the process of the phase rectification takes the comparison results over many clock-pulse cycles, e.g. several hundreds of the clock-pulse cycles, in order to achieve the phase needed. Thus, a longer lock-time is required. (2) The second one is phase noise: when the noise interferes with the input voltage of the voltage-controlled oscillator of the phase-lock loop circuit, frequency drift, i.e. phase noise, occurs. When clock-pulse is recovering, comparison of phases also depends on sequence of the received data stream. If the input signal is a long and same logical signal, the phase detector will not operate because no rising or falling edge occurs for the input signal. In such condition, the phase-lock loop circuit is unable to maintain the phase-lock state and the frequency may start to drift, resulting in the phase noise, as can be indicated in the frequency spectrum. (3) The third is only one receiving channel available. Only one receiving channel can be provided when we achieve the clock-pulse recovery by using the phase-lock loop circuit. Regarding a plurality of receiving channels, more phase-lock loop circuits are required for the clock-pulse recovery.

Therefore, using multiphase systems for data-recovery systems has become a trend nowadays. Since multi-phases may be distributed in one

clock-pulse period, the above mentioned phase-lock process can be achieved by selecting a suitable sampling clock-pulse. Not only phase-lock time is shorter, a phase-lock loop circuit can be provided for use with a plurality of receiving channels. There are several methods to generate multiphase signals. (1) The first one is delay-Lock loop. A long series of delay chain, such as two inverters connected in serial, is used for generating clock-pulse signals having different delay durations so as to form the multiphase signals. The advantage for this method is the stability. However, it also incurs the requirements of lots of delay units for covering 360 degrees of clock-pulse phases. In design, this needs more consideration as to whether it is proper to apply this in view of the cost. In addition, power consumption and inevitable noise disturbance resulted from electrical power lines become the bottlenecks in design. (b) The second one is multiphase VCO. (3/28) Currently, the newly developed multiphase oscillators are able to generate refined differences of phases uniformly distributed within one clock-pulse. In addition, the number of the generated multiphase signals can be the power of two. However, one of the difficulties is to avoid the problem of the multiphase oscillator model. The circuit layout is also an important consideration for this method. (c) The phase interpolation. The phase interpolation is one of the ways to generate the multiphase signals. A middle phase can be output by inputting different phases. The way to use the phase interpolation is easier and is the trend for future technology.

The advantages of the phase interpolation in comparison with the

above mentioned prior-art techniques are following: (a) It won't be limited by the delay time of the delay unit to decide the distribution density of the multiphase. The multiphase density and number can be easily decided by phase interpolation. The cost and the decaying power will balance in the design. The system is also very stable. (b) There is no disadvantage of the multi-oscillating model. And the number of the phases will increase by doubling the number of the input phase after the interpolation. For example, we can interpolate 8 phases once if we need 16 phases. ($8 \times 2 = 16$) If we need 20 phases then we can interpolate 10 phases once. ($10 \times 2 = 20$) Or, to interpolate 5 phases twice can also obtain the same result. The design is very free. (c) Because the phase-interpolation can produce the local multiphase clock signals by using fewer phases of the globe clock signals, therefore the area of the wiring and the number of the clock-pulse buffers will be fewer than the decay-lock-loop circuit and the multiphase oscillator in the application of the multi-receiving channels.

Conventional phase-interpolation methods include the type of non-full swing signal and the type of full swing signal. The phase-interpolation of the non-full swing signal type generally employs the V-to-I current adder. The middle phase can be generated by adding two signals with two different phases. A set of binary code or temperature code is applied to control the tail current of the circuit and to rectify the weighting of the adding signals. As a result, the phase of the interpolation produced can be controlled to drift backward or forward. The distribution of the phase is not distributed in one

clock-pulse period uniformly because the phase of the interpolation of the analog signal is decided by the rating of the tail current of the current adder.

The switch of the phase boundary is non-seamless. We have to get the analog signal near the position of the voltage-controlled oscillator for the phase interpolation because the input clock signal is non-full swing signal.

The result above will limit the application of the data-recovery system of the multi-receiving channel described above. The phase interpolation of the full swing signal will provide fewer globe clock signals of the phase to produce near local multiphase clock. The characteristic above is the advantage of the full swing signal type.

The disadvantages of the phase-interpolation method in the type of conventional full swing signal type include: (a) The decaying power of the short-circuit current is large. (b) The nonlinear phase distribution. (c) The duty cycle of the clock-pulse output is not 50%. The phase-interpolation circuit of the full swing signal type in prior art is composed of two inverters 11 and 12 as which shown in FIG. 1A. In addition, the inverters are composed of the complementary metal-oxide semiconductor (CMOS) devices, as which illustrated in FIG. 1B. The principle of the operation of the devices is to provide two-level clock signals CK1 and CK2. As shown in FIG. 1C, the phase of CK1 is before the phase of CK2 in order to produce an output signal with middle phase by short-circuit of the two inverters. However, as indicated by the arrow shown in FIG. 1B, the circuit will produce a short-circuit current I_{sc} when the time is T1 and T2 and when the double-level clock signal

CK1 is in the input end 111 and the double-level clock signal CK2 is in the input end 121. The disadvantage of large decaying power in the circuit exists. Besides, the phase of the interpolation signal produced cannot be controlled in the middle range of the phase of the original signals.

5 Please refer to FIG. 1D which is a schematic diagram illustrating an improved prior art circuit employing the above mentioned method. The circuit shown in FIG. 1D can correct the defects of the phase of the interpolation signal to be in the middle of the two original phases by fine tuning the current ratio of both discharging paths (e.g., to control the ratio of
10 tail current). However, such kind of method can only improve the linearity of the distribution of the phase by means of the ratio of current (e.g., W and $1-W$ shown in FIG. 1D), which is difficult to be controlled concisely. This method cannot achieve the yield of the mass production and cannot maintain the duty cycle of the original clock-pulse. It will require an additional duty cycle
15 correction circuit to maintain the 50% duty cycle.

FIG. 2A describes another prior art circuit, in which a phase-interpolation circuit that can avoid short-circuit current is provided. However, it also incurs the drawback of being only able to produce the interpolation phase for the falling edges of the clock pulses, but cannot
20 provide the interpolation phase for both the rising and falling edges of the clock pulses (as which shown in FIG. 2B). Therefore, such kind of circuit can only be used for doubling the frequency of multiphase clock pulse and it

will not produce a new middle phase for the doubled frequency; a phase alignment circuit that is formed by using the phase-interpolation circuit is also limited to the application for doubling the frequency of multiphase clock pulse. The primary object of the present invention is to improve the deficiencies of the above mentioned conventional phase-interpolation circuits. A full swing signal type phase-interpolation circuit will be provided which can avoid short-circuit current and provide linearly distributed multiphase clock pulses, which maintain good 50% duty cycle. In addition, we do not have to design additional duty cycle correction circuit. Moreover, we will be able to interpolate new middle phase between both the rising and falling edges of the clock pulse

SUMMARY OF THE INVENTION

The invention is directed to a phase-interpolation circuit capable of outputting a third double-level clock signal after a first double-level clock signal and a second double-level clock signal are inputted and processed, wherein when there is phase difference between the first and second double-level clock signals, the first double-level clock signal leads the second double-level clock signal, the circuit comprising: a first inverter, an input end of which is for receiving the first double-level clock signal; a second inverter, an input end of which is for receiving the second double-level clock signal and an output end of which is connected to an output end of the first inverter to form a common output end; a first controlled switch connected among the

first inverter, the second inverter, and a power source, wherein when the first double-level clock signal is in a high-level state, the first controlled switch becomes off, and when the first double-level clock signal is in a low-level state, the first controlled switch becomes on; and a second controlled switch
5 connected among the first inverter, the second inverter, and a ground point, wherein when the first double-level clock signal is in the high-level state, the second controlled switch becomes on, and when the first double-level clock signal is in the low-level state, the second controlled switch becomes off.

According to the above concept, the phase-interpolation circuit further
10 includes a third inverter, an input end of which is connected to the common output end and has an output end for outputting the third double-level clock signal.

According to the above concept, the phase-interpolation circuit further includes: a fourth inverter, an output end of which is connected to the first
15 inverter in order to output the first double-level clock signal to the input end of the first inverter; and a fifth inverter, an output end of which is connected to the second inverter in order to output the second double-level clock signal to the input end of the second inverter.

According to the above concept, in the phase-interpolation circuit, the
20 first controlled switch includes: a first p-channel metal-oxide semiconductor (PMOS), connected between the first inverter and the power source, the first

PMOS being off when the double-level clock signal is in the high-level state, and being on when the double-level clock signal is in the low-level state; and a second PMOS connected between the second inverter and the power source, the second PMOS being off when the double-level clock signal is in the high-level state, and being on when the double-level clock signal is in the low-level state.

According to the above concept, in the phase-interpolation circuit, the second controlled switch includes: a first n-channel metal-oxide semiconductor (NMOS) connected between the first inverter and the ground, the first NMOS being off when the double-level clock signal is in the low-level state, and being on when the double-level clock signal is in the high-level state; and a second NMOS connected between the second inverter and the ground point, the second NMOS being off when the double-level clock signal is in the low-level state, and being on when the double-level clock signal is in the high-level state.

According to the above concept, in the phase-interpolation circuit, the first controlled switch is a PMOS, connected among the first inverter, the second inverter, and the power source, the first controlled switch becomes off when the double-level clock signal is in the high-level state, and becomes on when the double-level clock signal is in the low-level state.

According to the above concept, in the phase-interpolation circuit, the

second controlled switch is an NMOS, connected among the first inverter, the second inverter, and the ground point, the second controlled switch becomes off when the double-level clock signal is in the low-level state, and becomes on when the double-level clock signal is in the high-level state.

5 According to the above concept, in the phase-interpolation circuit, the inverters are implemented by CMOS inverters.

Another aspect of the invention is directed to a phase-interpolation signal generating device for outputting a third double-level clock signal and a fourth double-level clock signal after a first double-level clock signal and a second double-level clock signal are inputted to and processed by the device, wherein there is a specific phase difference between the first double-level clock signal and the second double-level clock signal, the phase difference between the third and the fourth double-level clock signals is smaller than the specific value, the device comprises five phase-interpolation circuits, each phase-interpolation circuit comprises a first input end, a second input end, and an output end, an output signal outputted from the output end has its phase which is between phases of both input signals of the two input ends, wherein the phase-interpolation circuits comprises: a first phase-interpolation circuit, whose two input ends are for receiving the first double-level clock signal; a second phase-interpolation circuit, whose two input ends are respectively for receiving the first double-level clock signal and the second double-level clock signal; a third phase-interpolation circuit, whose two input

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ends are for receiving the second double-level clock signal; a fourth phase-interpolation circuit, whose two input ends are separately connected to the output ends of the first and the second phase-interpolation circuits respectively, and whose output end outputs the third double-level clock signal; and a fifth phase-interpolation circuit, whose two input ends separately connected to the output ends of the second and the third phase-interpolation circuits respectively, the output end of the fifth phase-interpolation circuit outputting the fourth double-level clock signal; wherein one phase-interpolation circuit of the phase-interpolation circuits comprises: a first inverter, whose input end is for receiving the double-level clock signal inputted from the first input end of the phase-interpolation circuit; a second inverter, whose input end is for receiving the double-level clock signal inputted from the second input end of the phase-interpolation circuit, wherein when there is a phase difference between the double-level clock signal inputted from the first input end and the double-level clock signal inputted from the second input end the first, the double-level clock signal inputted from the first input end leads the double-level clock signal inputted from the second input end the first, wherein an output end of the second inverter is connected to an output end of the first inverter to form a common output end; a first controlled switch, connected among the first inverter, the second inverter, and a power source, wherein the first controlled switch is off when the double-level clock signal inputted from the first input end is in a high-level state, and is on when the double-level clock signal inputted from the first

input end is in a low-level state; and a second controlled switch, connected between the first inverter, the second inverter, and a ground point, wherein the second controlled switch is on when the double-level clock signal inputted from the first input end is in the high-level state, and is off when the
5 double-level clock signal inputted from the first input end is in the low-level state.

According to the above concept, in the phase-interpolation signal generating device, each of the phase-interpolation circuits further comprises: a third inverter, whose input end is connected to the common output end of
10 the phase-interpolation circuit.

According to the above concept, in the phase-interpolation signal generating device, each of the phase-interpolation circuits further comprises: a fourth inverter, whose output end is connected to the input end of the first inverter; and a fifth inverter, whose output end is connected to the input end
15 of the second inverter.

According to the above concept, in the phase-interpolation signal generating device, the first controlled switch comprises: a first PMOS; connected between the first inverter and the power source, the first PMOS being off when the double-level clock signal is in the high-level state, and
20 being on when the double-level clock signal is in the low-level state; and a second PMOS, connected between the second inverter and the power source,

the second PMOS being off when the double-level clock signal is in the high-level state, and being on when the double-level clock signal is in the low-level state.

According to the above concept, in the phase-interpolation signal
5 generating device, the second controlled switch comprises: a first NMOS, connected between the first inverter and the ground point, the first NMOS being off when the double-level clock signal is in the low-level state, and being on when the double-level clock signal is in the high-level state; and a second NMOS, connected between the second inverter and the ground point,
10 the second NMOS being off when the double-level clock signal is in the low-level state, and being on when the double-level clock signal is in the high-level state.

According to the above concept, in the phase-interpolation signal
generating device, the first controlled switch is a PMOS, connected among
15 the first inverter, the second inverter, and the power source, the first controlled switch being off when the double-level clock signal is in the high-level state, and being on when the double-level clock signal is in the low-level state.

According to the above concept, in the phase-interpolation signal
20 generating device, the second controlled switch is an NMOS, connected among the first inverter, the second inverter, and the ground point, the second

controlled switch being off when the double-level clock signal is in the low-level state, and being on when the double-level clock signal is in the high-level state.

According to the above concept, in the phase-interpolation signal
5 generating device, the inverters are implemented by using a CMOS inverter.

According to the above concept, in the phase-interpolation signal generating device, the phase-interpolation circuits have the same structure.

According to the above concept, in the phase-interpolation signal generating device, the phase difference between the third double-level clock
10 signal and the fourth double-level clock signal is a half of the specific value.

BRIEF DESCRIPTION OF THE DRAWINGS

Deeper understanding of the invention will become apparent from the following accompanying drawings and detailed description. FIG. 1(a) is a
15 schematic diagram showing a conventional digital type phase-interpolation circuit. FIG. 1(b) is a schematic diagram showing a conventional phase-interpolation circuit in which its inverters are implemented by CMOS. FIG. 1(c) is a diagram illustrating the waveforms of the double-level clock signals CK1 and CK2 inputted to the conventional phase-interpolation circuit.
20 FIG. 1(d) is a schematic diagram showing a conventional phase-interpolation

circuit. FIG. 2(a) is a schematic diagram showing another conventional phase-interpolation circuit to avoid short-circuit current. FIG. 2(b) is a diagram illustrating the waveforms of the clock signals in the conventional phase-interpolation circuit shown in FIG. 2(a).

5 FIG. 3 illustrates a schematic diagram of a preferred embodiment of the phase-interpolation circuit according to the present invention. [Translator's notes: the translations of Chinese words accompanying the legends (i.e. 30-37, 311-312, 321-322 and 331) in the original FIG. 3 are listed in the following "BRIEF DESCRIPTION OF LEGENDS IN THE DRAWINGS" and
10 thus will not be repeated in the present drawing of FIG. 3 for the sake of brevity; a legend 321 at the left part of the original FIG. 3, pointing to an inverter, should be corrected as 37 (fifth inverter) according to the context.]

FIGS. 4(a) and 4(b) illustrate two circuit examples in which the controlled switch circuits are implemented by MOS. [Translator's notes: the translations
15 of Chinese words accompanying the legends (i.e. 33, 36 and 37) in the original FIGS. 4(a) and 4(b) are listed in the following "BRIEF DESCRIPTION OF LEGENDS IN THE DRAWINGS" and thus will not be repeated in the present drawing for the sake of brevity.]

FIG. 5 is a diagram illustrating the waveforms including the double-level clock
20 signal CK1 inputted to the phase-interpolation circuit and the double-level clock signal CK1-2 outputted by the phase-interpolation circuit.

FIG. 6 is a schematic diagram illustrating a preferred embodiment of the phase-interpolation signal generating device according to the present invention. [Translator's notes: the translations of Chinese words accompanying the legends (i.e. 61-65) in the original FIG. 6 are listed in the following "BRIEF DESCRIPTION OF LEGENDS IN THE DRAWINGS" and thus will not be repeated in the present drawing for the sake of brevity.]

FIGS. 7(a), 7(b), 7(c), 7(d), and 7(e) are diagrams showing the waveforms of the clock-pulse signals in the preferred embodiment as shown in FIG. 6.

FIG. 8 is a schematic diagram illustrating another embodiment of the phase-interpolation signal generating device according to the present invention which can generate eight output multiphase signals based on four input multiphase signals.

BRIEF DESCRIPTION OF LEGENDS IN THE DRAWINGS

Inverters 11, 12	Input ends 111, 121
First inverter 31	Input end 311
Output end 312	Second inverter 32
Input end 321	Output end 322
Common output end 30	Third converter 33
Input end 331	First controlled switch 34
Second controlled switch 35	First phase-interpolation circuit 61
Second phase-interpolation circuit 62	Third phase-interpolation circuit 63
Fourth phase-interpolation circuit 64	Fifth phase-interpolation circuit 65
Fourth inverter 36	Fifth inverter 37

DESCRIPTION OF PRFERRED EMBODIMENTS

Please refer to FIG. 3, which is a schematic diagram of a preferred embodiment of the phase-interpolation circuit of the present invention. The phase-interpolation circuit shown in FIG. 3 includes five inverters and two controlled switches. Specifically, the input end 311 of a first inverter 31 receives a phase-leading double-level clock signal CK1. The input end 321 of a second inverter 32 receives a phase-lagging double-level clock signal CK2. The output end 322 of the second inverter 32 is connected to the output end 312 of the first inverter 31 to form a common output end 30. The input end 331 of the third inverter 33 connects to the common output end 30 electrically. The output ends of a fourth inverter 36 and a fifth inverter 37 are connected to the input ends of the first inverter 31 and the second inverter 32 respectively.

In order to avoid short-circuit current, the embodiment of the invention further includes a first controlled switch 34 and a second controlled switch 35. The first controlled switch 34 is electrically connected among the first inverter 31, the second inverter 32, and the electrical power source (VDD). The first controlled switch 34 becomes off when the double-level clock signal CK1 is in a high-level state. The first controlled switch 34 becomes on when the double-level clock signal CK1 is in a low-level state. The second controlled

switch 35 is electrically connected among the first inverter 31, the second inverter 32, and the ground (GND). The second controlled switch 35 becomes on when the double-level clock signal CK1 is in the high-level state. The second controlled switch 35 becomes off when the double-level clock signal CK1 is in the low-level state. In the above example, the phase-leading double-level clock signal CK1 is used to control the timing of the open or closed states of the controlled switches 34 and 35, thereby avoiding short-circuit current.

Please refer to FIGS. 4(a) and 4(b), which are circuit embodiments wherein the inverters are implemented by using CMOS inverters and the controlled switches are implemented by using MOS transistors. In the following description, "1" represents the high-level state and "0" represents the low-level state for the sake of illustration. The states of (CK1, CK1) changing from (0,0), (1,0) to (1,1) are discussed. [Translator's note: (CK1, CK1) should be corrected and read as (CK1, CK2) according to the original context.] When CK1 rises from "0" to "1", it indicates that the lagging clock signal CK2 will also rise (still as "0" then). In the same time, the common output end 30 is going to fall from "1" to "0". When CK1="1", the PMOS in the controlled switch will be off and the NMOS in the controlled switch will be on. Since the VDD has been disconnected, the short-circuit current, as happened conventionally, will not occur even when (CK1, CK2) become (1,0) in which the NMOS of the first inverter 31 and the PMOS of the second inverter 32 are on to form a short-circuit path. In addition, the function of the

common output end 30 also meets the need of phase-interpolation since the stray capacitor thereof will discharge to "0" gradually. In an opposite situation, (CK1, CK2) are changing from (1,1), (0,1) to (0,0). When the CK1 falls down to "0", it indicates that the lagging clock signal CK2 will also fall
5 down (still as "1" then). In the same time, the common output end will rise from "0" to "1". When CK1="0", the PMOS will be on and the NMOS will be off. Since the connection toward GND has been off, the short-circuit current, as happened conventionally, will not occur even when (CK1, CK2) become (0,1), the PMOS of the first inverter 31 and the NMOS of the second inverter
10 32 are both on to form a short-circuit path therebetween. In addition, the common output end 30 meets the requirements of the phase-interpolation function because the stray capacitor will charge to "1" gradually. The signal comes from the common output end 30 will be further processed by the third inverter 33 so as to output a double-level clock signal CK1-2, as shown in FIG.
15 5, having its phase between those of CK1 and CK2. Since the phase-interpolation circuit according to this embodiment of the invention avoids the occurrence of short-circuit current during mixing phases by using switches disposed between VDD and GND, which are controlled by phase-leading clock signal CK1, the problem of power dissipation can be
20 effectively improved.

However, since the middle phase signal is generated by the charging/discharging processes of the capacitors of different inverters controlled by different clock pulses with different phases, the middle phase

signal might drift toward one of the neighbor phases (e.g., P1 is unequal to P2 in FIG. 5) if the charging/discharging ability is imbalance and the ratio of charging/discharging current to the capacitance is improper. As a result, the ideal 50% duty cycle may drift. The error of the middle phase might be smaller than 3% if suitable parameters are adjusted. However, many uncertainties such as changing of temperature, manufacturing error and stray capacitors may still make the middle phase to drift away from the ideal value. To resolve this problem, the present invention discloses a phase-interpolation signal generation device according a preferred embodiment in a block diagram, as shown in FIG. 6. The device includes five phase-interpolation circuits. Each phase-interpolation circuit can be implemented by using the circuit illustrated in FIG. 3. These five phase-interpolation circuits include the first phase-interpolation circuit 61, the second phase-interpolation circuit 62, the third phase-interpolation circuit 63, the fourth phase-interpolation circuit 64 and the fifth phase-interpolation circuit 65. Both input ends of the first phase-interpolation circuit 61 receive the first double-level clock signal CK0. The two input ends of the second phase-interpolation circuit 62 receive the first double-level clock signal CK0 and the second double-level clock signal CK1 respectively. Both of the two input ends of the third phase-interpolation circuit 63 receive the second double-level clock signal CK1. The two input ends of the fourth phase-interpolation circuit 64 are separately connected to the output ends of the first phase-interpolation circuit 61 and the second phase-interpolation circuit 62, respectively. The output

end of the fourth phase-interpolation circuit 64 outputs the third double-level clock signal CK2-0. The two input ends of the fifth phase-interpolation circuit 65 are respectively connected to the output ends of the second phase-interpolation circuit 62 and the third phase-interpolation circuit 63.

- 5 The output end of the fifth phase-interpolation circuit 65 outputs the fourth double-level clock signal CK2-1.

The waveforms shown in FIG. 7(a) schematically illustrate an example of the first double-level clock signal CK0 and the second double-level clock signal CK1. FIG. 7(b) illustrates the signal of the common output end 30 of the first-stage phase-interpolation circuit. For some uncertainties as mentioned above, the middle phase might drift as shown in FIG. 7(b). The middle phase obtained after the process of the third inverter 33 is shown in FIG. 7(c). The signal of the common output end 30 in the second-stage phase-interpolation circuit connected is shown in FIG. 7(d). Since the clock pulse is processed by two stages of same phase-interpolation circuits, the leading and lagging clock pulses are in the same process of the leading and lagging paths and the interpolation of the phases are also in the same process of the phase-interpolation circuit for the rising and falling edges. Therefore, unbalanced effect of the NMOS and PMOS and different delay paths of the circuit are averaged to compensate for the non-linearity of the phase distribution. As shown in FIG. 7(e), the output waveforms of the third double-level clock signal CK2-0 and the fourth double-level clock signal CK2-1 will have phases uniformly distributed within a period of clock pulse.

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Experimental simulation indicates that the error of the linear distribution of the phase will be smaller than 0.1%. Due to the inversion characteristics of the phase-interpolation, the phase-interpolation circuit that processes the signal in the rising and falling edges also corrects the 50% duty cycle of the output clock pulse at the same time. Experimental simulation indicates that if it is designed appropriately, the error of the duty cycle will be smaller than 1% and will not be drifted by manufacturing parameters. The linearity of the phase-interpolation distribution and the 50% duty cycle of the clock signal can be improved by using the phase-interpolation module and the phase averaging module, thereby broadening the range of their practical applications.

FIG. 8 is a schematic diagram illustrating another embodiment of the phase-interpolation signal generating device of the present invention which can generate eight output multiphase signals based on four input multiphase signals. Therefore, various modifications and similar arrangements can be made by one skilled in the art according to the invention, but are still within the scope to be protected, as indicated by the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1(a) is a schematic diagram showing a conventional digital type phase-interpolation circuit.

FIG. 1(b) is a schematic diagram showing a conventional phase-interpolation circuit in which its inverters are implemented by CMOS.

FIG. 1(c) is a diagram illustrating the waveforms of the double-level clock signals CK1 and CK2 inputted to the conventional phase-interpolation circuit.

FIG. 1(d) is a schematic diagram showing a conventional phase-interpolation circuit.

FIG. 2(a) is a schematic diagram showing another conventional phase-interpolation circuit to avoid short-circuit current.

FIG. 2(b) is a diagram illustrating the waveforms of the clock signals in the conventional phase-interpolation circuit shown in FIG. 2(a).

FIG. 3 illustrates a schematic diagram of a preferred embodiment of the phase-interpolation circuit according to the present invention.

FIGS. 4(a) and 4(b) illustrate two circuit examples in which the controlled switch circuits are implemented by MOS.

FIG. 5 is a diagram illustrating the waveforms including the double-level clock signal CK1 inputted to the phase-interpolation circuit and the double-level clock signal CK1-2 outputted by the phase-interpolation circuit.

FIG. 6 is a schematic diagram illustrating a preferred embodiment of the
5 phase-interpolation signal generating device according to the present invention.

FIGS. 7(a), 7(b), 7(c), 7(d), and 7(e) are diagrams showing the waveforms of the clock-pulse signals in the preferred embodiment as shown in FIG. 6.

FIG. 8 is a schematic diagram illustrating another embodiment of the
10 phase-interpolation signal generating device according to the present invention which can generate eight output multiphase signals based on four input multiphase signals.

VI. WHAT IS CLAIMED IS:

1. A phase-interpolation circuit capable of outputting a third double-level clock signal after a first double-level clock signal and a second double-level clock signal are inputted and processed, wherein when there is phase
5 difference between the first and second double-level clock signals, the first double-level clock signal leads the second double-level clock signal, the circuit comprising:

a first inverter, an input end of which is for receiving the first double-level clock signal;

10 a second inverter, an input end of which is for receiving the second double-level clock signal and an output end of which is connected to an output end of the first inverter to form a common output end;

a first controlled switch, connected among the first inverter, the second inverter, and a power source, wherein when the first double-level clock signal
15 is in a high-level state, the first controlled switch becomes off, and when the first double-level clock signal is in a low-level state, the first controlled switch becomes on; and

a second controlled switch, connected among the first inverter, the second inverter, and a ground point, wherein when the first double-level clock
20 signal is in the high-level state, the second controlled switch becomes on,

and when the first double-level clock signal is in the low-level state, the second controlled switch becomes off.

2. The phase-interpolation circuit as in claim 1, further comprising a third inverter, an input end of which is connected to the common output end and
5 has an output end for outputting the third double-level clock signal.

3. The phase-interpolation circuit as in claim 1, further comprising:

a fourth inverter, an output end of which is connected to the first inverter in order to output the first double-level clock signal to the input end of the first inverter; and

- 10 a fifth inverter, an output end of which is connected to the second inverter in order to output the second double-level clock signal to the input end of the second inverter.

4. The phase-interpolation circuit as in claim 1, wherein the first controlled switch comprises:

- 15 a first PMOS, connected between the first inverter and the power source, the first PMOS being off when the double-level clock signal is in the high-level state, and being on when the double-level clock signal is in the low-level state; and

a second PMOS connected between the second inverter and the

power source, the second PMOS being off when the double-level clock signal is in the high-level state, and being on when the double-level clock signal is in the low-level state.

5 5. The phase-interpolation circuit as in claim 1, wherein the second controlled switch comprises:

 a first NMOS connected between the first inverter and the ground, the first NMOS being off when the double-level clock signal is in the low-level state, and being on when the double-level clock signal is in the high-level state; and

10 a second NMOS connected between the second inverter and the ground point, the second NMOS being off when the double-level clock signal is in the low-level state, and being on when the double-level clock signal is in the high-level state.

15 6. The phase-interpolation circuit as in claim 1, wherein the first controlled switch is a PMOS, connected among the first inverter, the second inverter, and the power source, the first controlled switch becomes off when the double-level clock signal is in the high-level state, and becomes on when the double-level clock signal is in the low-level state.

20 7. The phase-interpolation circuit as in claim 1, wherein the second controlled switch is an NMOS, connected among the first inverter, the second

inverter, and the ground point, the second controlled switch becomes off when the double-level clock signal is in the low-level state, and becomes on when the double-level clock signal is in the high-level state.

8. The phase-interpolation circuit as in one of claims 1, 2, and 3, wherein
5 the inverters are implemented by CMOS inverters.
9. A phase-interpolation signal generating device for outputting a third double-level clock signal and a fourth double-level clock signal after a first double-level clock signal and a second double-level clock signal are inputted to and processed by the device, wherein there is a specific phase difference
10 between the first double-level clock signal and the second double-level clock signal, the phase difference between the third and the fourth double-level clock signals is smaller than the specific value, the device comprises five phase-interpolation circuits, each phase-interpolation circuit comprises a first input end, a second input end, and an output end, an output signal outputted
15 from the output end has its phase which is between phases of both input signals of the two input ends, wherein one phase-interpolation circuit of the phase-interpolation circuits comprises: [Translator's note: from the context, the phrase "one phase-interpolation circuit of the phase-interpolation circuits comprises" should be corrected as the phase-interpolation signal generating
20 device comprises]

a first phase-interpolation circuit, whose two input ends are for

receiving the first double-level clock signal;

a second phase-interpolation circuit, whose two input ends are respectively for receiving the first double-level clock signal and the second double-level clock signal;

5 a third phase-interpolation circuit, whose two input ends are for receiving the second double-level clock signal;

a fourth phase-interpolation circuit, whose two input ends are separately connected to the output ends of the first and the second phase-interpolation circuits respectively, and whose output end outputs the
10 third double-level clock signal; and

a fifth phase-interpolation circuit, whose two input ends separately connected to the output ends of the second and the third phase-interpolation circuits respectively, the output end of the fifth phase-interpolation circuit outputting the fourth double-level clock signal; wherein each of the
15 phase-interpolation circuits further comprises:

a first inverter, whose input end is for receiving the double-level clock signal inputted from the first input end of the phase-interpolation circuit;

a second inverter, whose input end is for receiving the double-level clock signal inputted from the second input end of the phase-interpolation
20 circuit, wherein when there is a phase difference between the double-level

clock signal inputted from the first input end and the double-level clock signal inputted from the second input end the first, the double-level clock signal inputted from the first input end leads the double-level clock signal inputted from the second input end the first, wherein an output end of the second
5 inverter is connected to an output end of the first inverter to form a common output end;

a first controlled switch, connected among the first inverter, the second inverter, and a power source, wherein the first controlled switch is off when the double-level clock signal inputted from the first input end is in a high-level
10 state, and is on when the double-level clock signal inputted from the first input end is in a low-level state; and

a second controlled switch, connected between the first inverter, the second inverter, and a ground point, wherein the second controlled switch is on when the double-level clock signal inputted from the first input end is in
15 the high-level state, and is off when the double-level clock signal inputted from the first input end is in the low-level state.

10. The phase-interpolation signal generating device as in claim 9, wherein each of the phase-interpolation circuits further comprises: a third inverter, whose input end is connected to the common output end of the
20 phase-interpolation circuit.

11. The phase-interpolation signal generating device as in claim 9, wherein

each of the phase-interpolation circuits further comprises:

a fourth inverter, whose output end is connected to the input end of the first inverter; and

a fifth inverter, whose output end is connected to the input end of the second inverter.

12. The phase-interpolation signal generating device as in claim 9, wherein the first controlled switch comprises:

a first PMOS, connected between the first inverter and the power source, the first PMOS being off when the double-level clock signal is in the high-level state, and being on when the double-level clock signal is in the low-level state; and

a second PMOS, connected between the second inverter and the power source, the second PMOS being off when the double-level clock signal is in the high-level state, and being on when the double-level clock signal is in the low-level state.

13. The phase-interpolation signal generating device as in claim 9, wherein the second controlled switch comprises:

a first NMOS, connected between the first inverter and the ground point, the first NMOS being off when the double-level clock signal is in the

low-level state, and being on when the double-level clock signal is in the high-level state; and

a second NMOS, connected between the second inverter and the ground point, the second NMOS being off when the double-level clock signal is in the low-level state, and being on when the double-level clock signal is in the high-level state.

14. The phase-interpolation signal generating device as in claim 9, wherein the first controlled switch is a PMOS, connected among the first inverter, the second inverter, and the power source, the first controlled switch being off when the double-level clock signal is in the high-level state, and being on when the double-level clock signal is in the low-level state.

15. The phase-interpolation signal generating device as in claim 9, wherein the second controlled switch is an NMOS, connected among the first inverter, the second inverter, and the ground point, the second controlled switch being off when the double-level clock signal is in the low-level state, and being on when the double-level clock signal is in the high-level state.

16. The phase-interpolation signal generating device as in one of claims 9, 10, and 11, wherein the inverters are implemented by a CMOS inverter.

17. The phase-interpolation signal generating device as in claim 8, wherein the phase-interpolation circuits have the same structure.

18. The phase-interpolation signal generating device as in claim 8, wherein the phase difference between the third double-level clock signal and the fourth double-level clock signal is a half of the specific value.

[Translator's note: according to the subject matter of claims 17 and 18, they

5 should depend from claim 9, for example, rather than claim 8.]

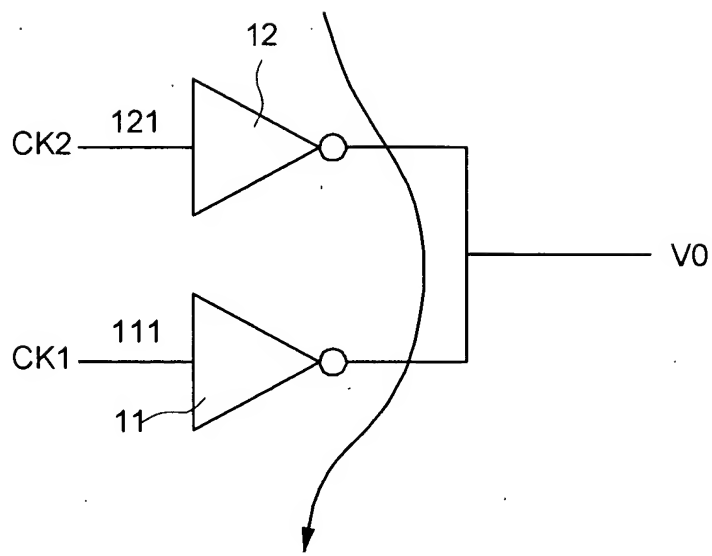


FIG.1(a)

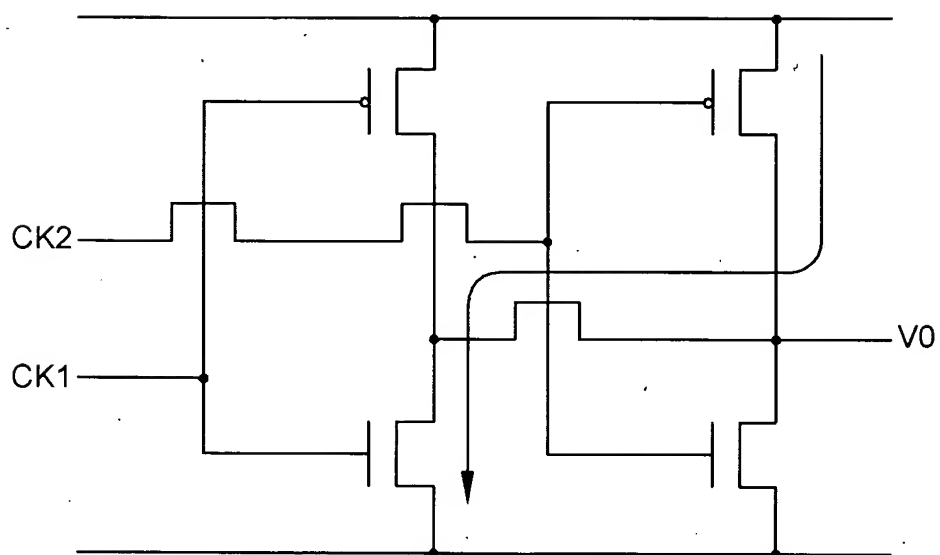


FIG.1(b)

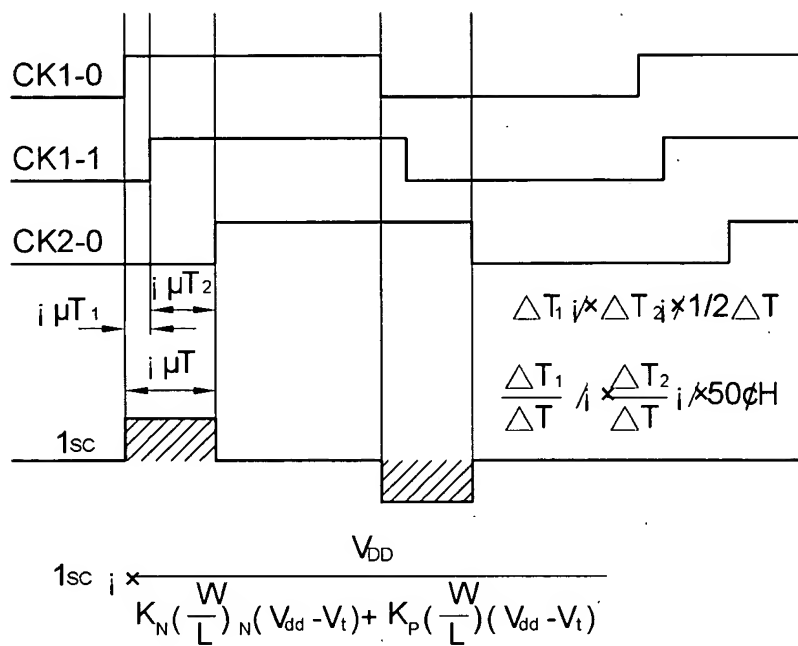


FIG.1(c)

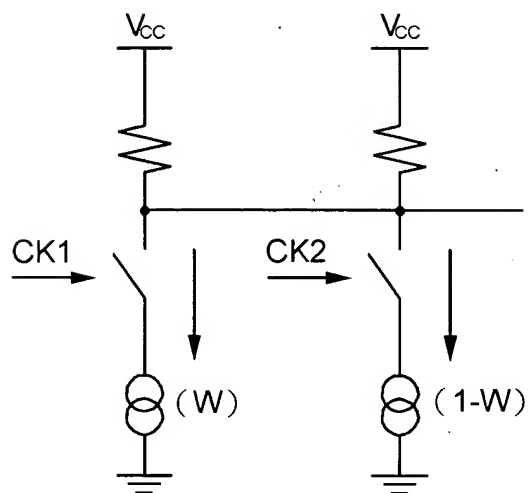


FIG.1(d)

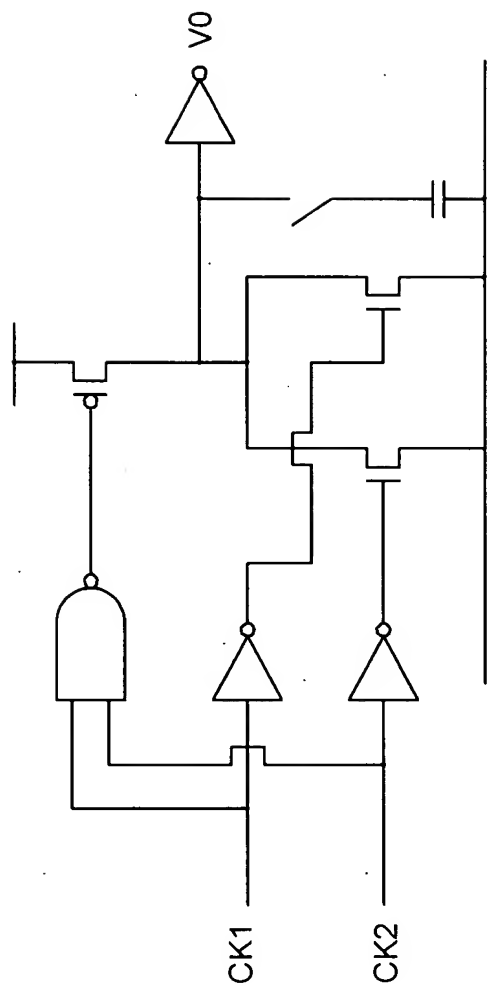


FIG. 2(a)

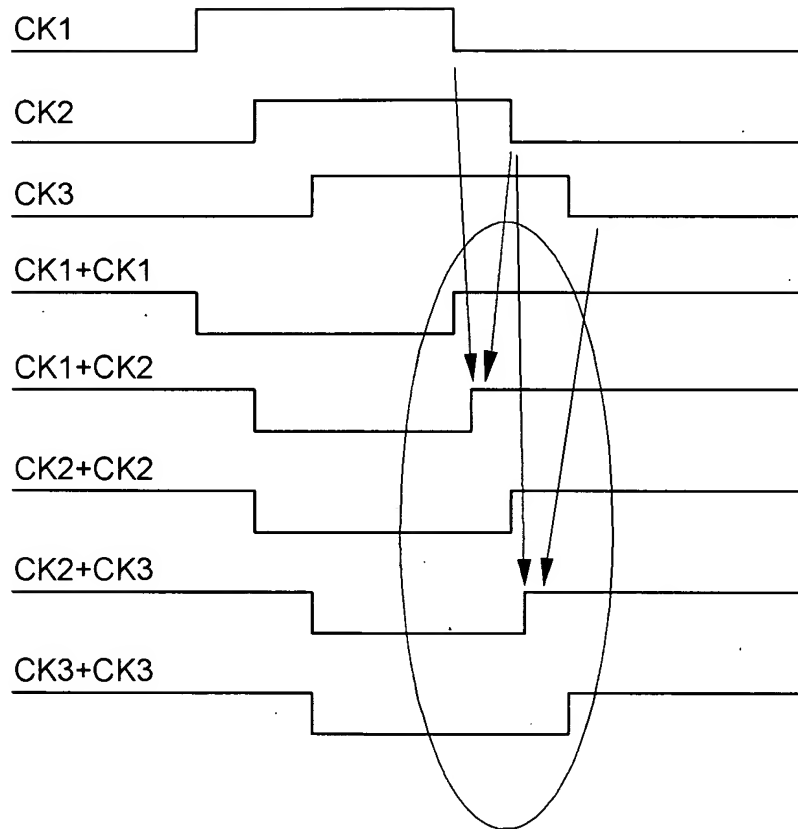


FIG.2(b)

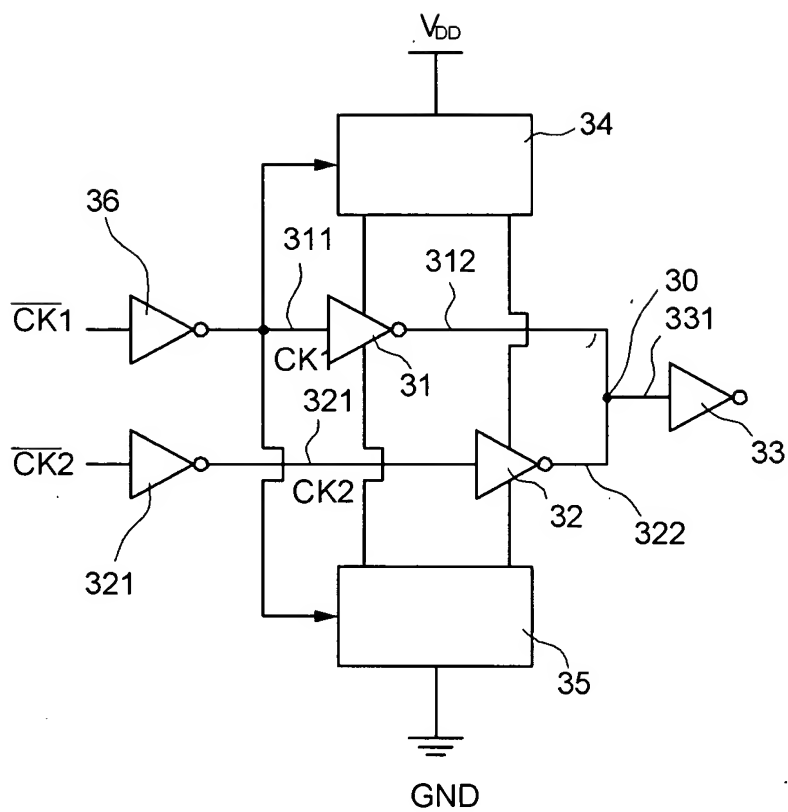


FIG.3

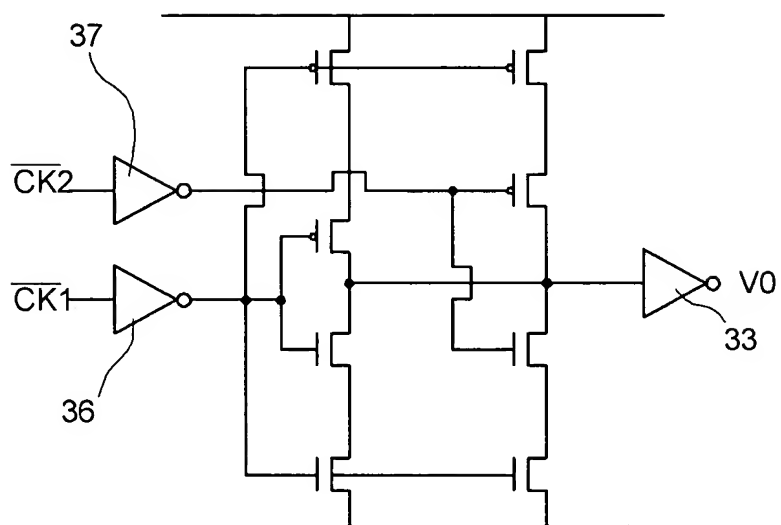


FIG.4(a)

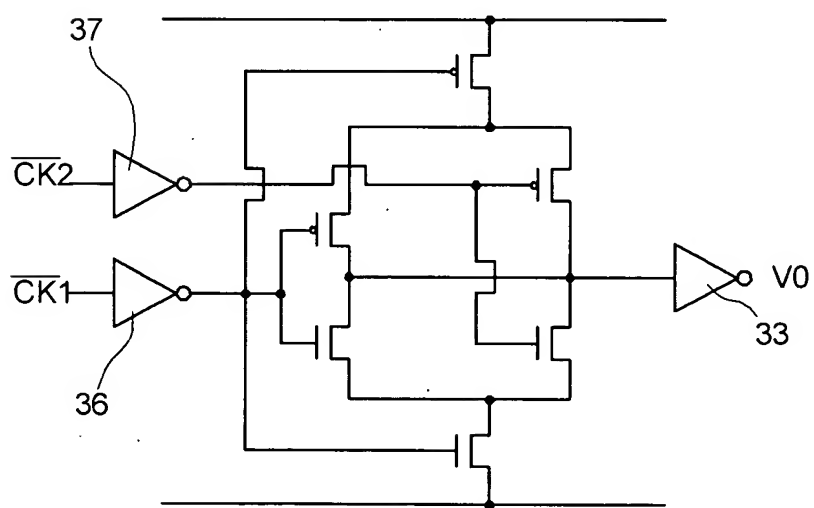


FIG.4(b)

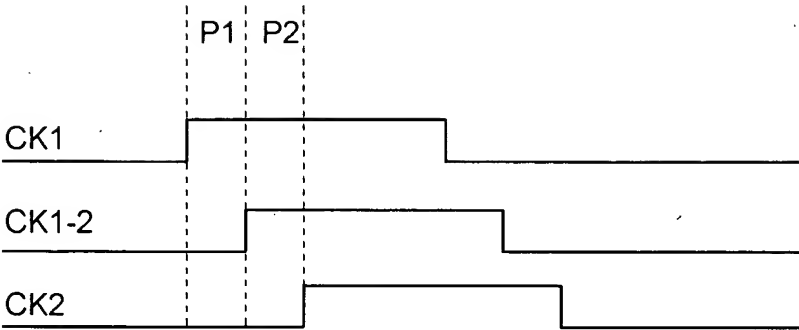


FIG.5

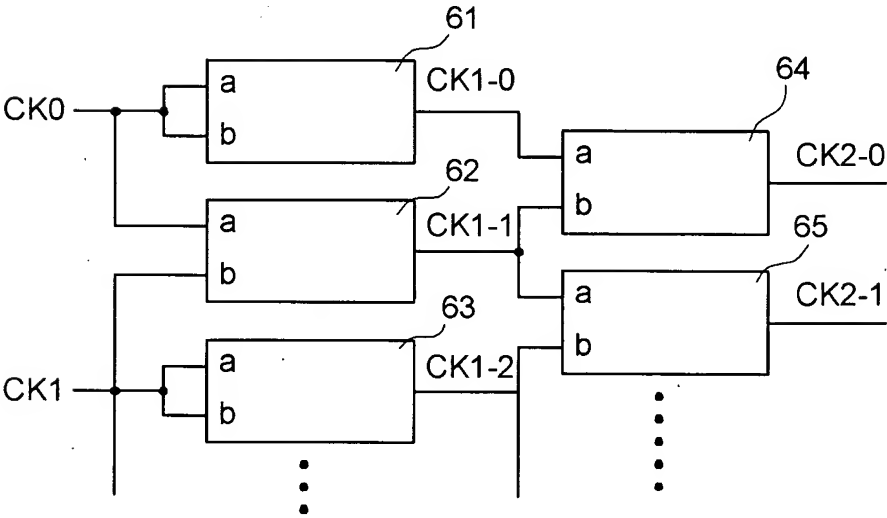


FIG.6

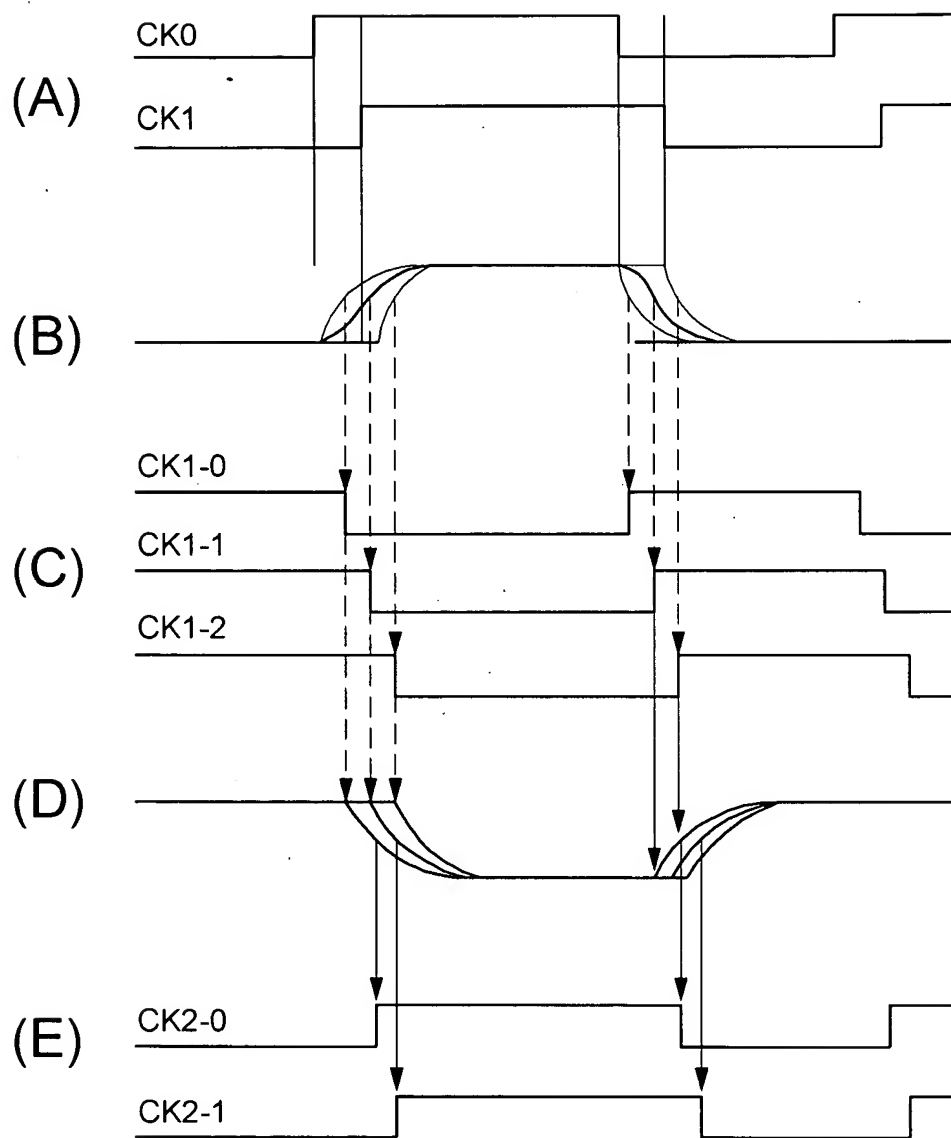


FIG.7

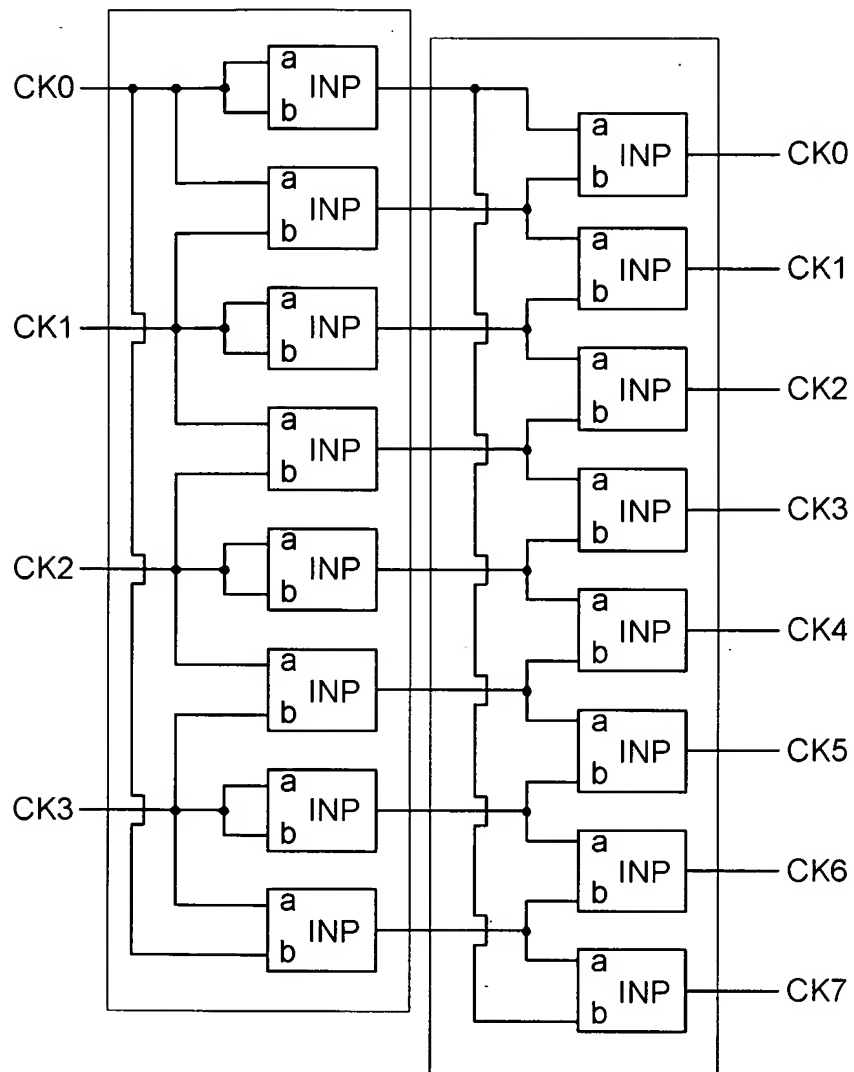


FIG.8